A NEW METHOD FOR DETERMINING THE FET SMALL SIGNAL EQUIVALENT CIRCUIT

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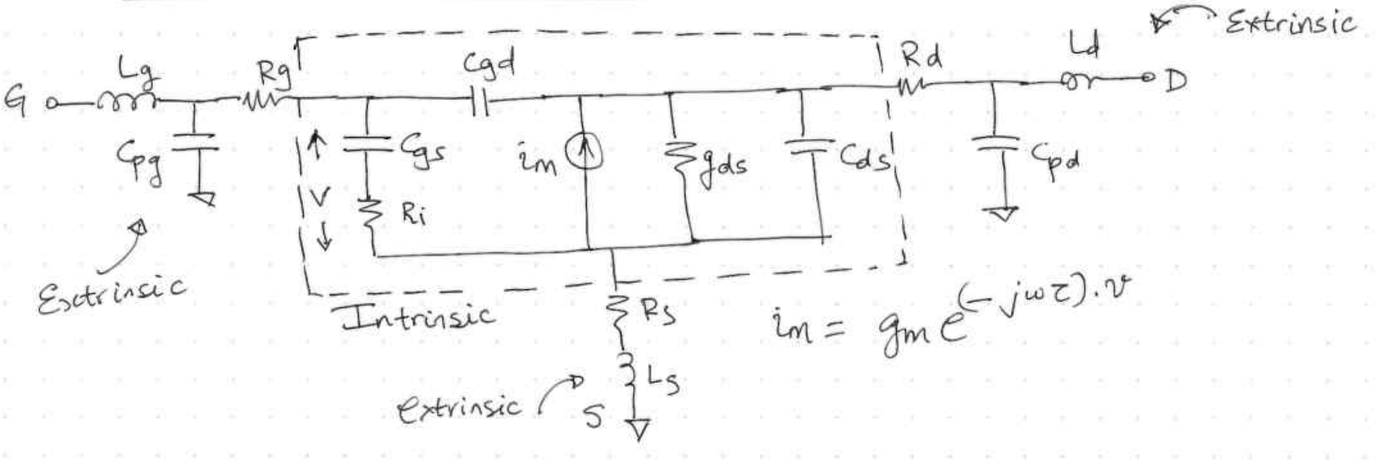
This paper describes how to extract all the elements of a small signal model of a FET, by making s-parameter measurements at relatively low frequency. The resulting s-parameter model is valid upto even 26.5GHz.

SMALL SIGNAL EQVT. CIRCUIT



$i_m = g_m e^{(-j\omega\tau)} . v$

The Y-parameters of the intrinsic device are:

$$y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \quad \text{---(1)}$$

$$y_{21} = \frac{g_m e^{-j\omega\tau}}{1 + jR_i C_{gs}\omega} - j\omega C_{gd} \quad \text{--(3)}$$

$$y_{12} = -j\omega C_{gd} \quad \text{---(2)}$$

$$y_{22} = g_d + j\omega(C_{ds} + C_{gd}) \quad \text{--(4)}$$

with $D = 1 + \omega^2 C_{gs}^2 R_i^2$

For a typical low noise device, $\omega^2 C_{gs}^2 R_i^2 < 0.01$ at $f < 5\,GHz$ so $D \approx 1$. In addition, assume $\omega\tau << 1$

$$y_{11} = R_i C_{gs}^2 \omega^2 + j\omega(C_{gs} + C_{gd}) \quad \text{---(5)}$$

$$y_{21} = g_m - j\omega(C_{gd} + g_m(R_i C_{gs} + \tau)) \quad \text{--(7)}$$

$$y_{12} = -j\omega C_{gd} \quad \text{--(6)}$$

$$y_{22} = g_d + j\omega(C_{ds} + C_{gd}) \quad \text{--(8)}$$

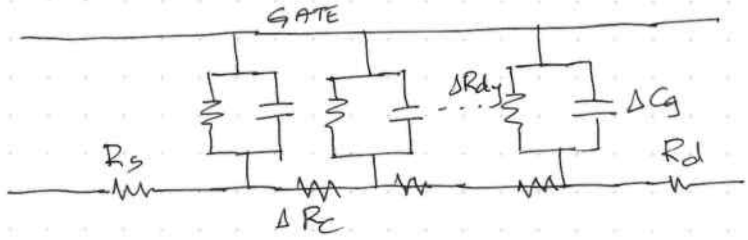
So, the method to extract all small signal parameters is:

1) Find C_{gd} from y_{12}
2) Use C_{gd} from (1) in y_{11} and find R_i and C_{gs}
(3) Use C_{gd}, R_i, C_{gs} in y_{21} and find g_m and τ
(4) Use C_{gd} from y_{12} in y_{22} and find g_{ds} and C_{ds}

But to get the y-parameters of the intrinsic device, the external / extrinsic elements need to be known.
Usually, on-wafer, this is not an issue ~~do~~ due to open-Short de-embedding, so this is not particularly important the know the values of extrinsic elements. But, the method is still good to know. (There may be feed line effects still)

MEASUREMENT OF EQUIVALENT CIRCUIT ELEMENTS THAT ARE EXTRINSIC

- Extraction is done with $V_{DS} = 0$, aka, COLDFET because the equivalent circuit is simpler, as shown below:



For any gate biasing conditions,

$$z_{11} = R_c/3 + z_{dy} \quad \text{--- (9)}$$
$$z_{12} = z_{21} = R_c/2 \quad \text{--- (10)}$$
$$z_{22} = R_c \quad \text{--- (11)}$$

$R_c \rightarrow$ Channel resistance
$z_{dy} \rightarrow$ eqnt impedance of schottky barrier

$$z_{dy} = \frac{R_{dy}}{1 + j\omega C_g R_{dy}}, \quad R_{dy} = \frac{nKT}{q I_g} \quad \text{-- (12)}$$

As gate current increases, R_{dy} decreases and C_g increases but R_{dy} decreases rapidly with ~~C_{gs}~~ V_{gs} $\Rightarrow$ $\omega R_{dy} C_g \to 0$ for high gate current densities, then.

$$z_{dy} = R_{dy} = \frac{nKT}{q I_g} \quad \text{---(13)}$$

for large gate current, capacitive effect of gate disappears, $z_{11} \to$ real:

$$z_{11} = R_c/3 + \frac{nKT}{q I_g} \quad \text{--(14)}$$

To get extrinsic Z parameters, parasitic R/L is added to intrinsic z parameters:

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nKT}{q I_g} + j\omega(L_s + L_g) \quad \text{-.(15)}$$

$$Z_{12} = Z_{21} = R_s + R_c/2 + j\omega L_s \quad \text{---(16)}$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d) \quad \text{---(17)}$$

The imaginary parts of these equations linearly increases with freq. The real parts are freq independent. But $Re(Z_{11}) \propto \frac{1}{I_g}$

Now, parasitics are easy to extract.

$Im(Z_{12}) = Im(Z_{21}) \rightarrow$ gives L_s

$Im(Z_{22})$ & L_s $\rightarrow$ gives L_d

$Im(Z_{11})$ & L_s $\rightarrow$ gives L_g

The ordinate of plot of $Re(Z_{11})$ vs $\frac{1}{I_g}$ gives $R_s + R_g + \frac{R_c}{3}$

$Re(Z_{12}) = Re(Z_{21})$ gives $R_s + R_c/2$

$Re(Z_{22})$ = gives $R_s + R_d + R_c$

4 unknowns
3 relations.

Rs can also be determined by Yang Long Method

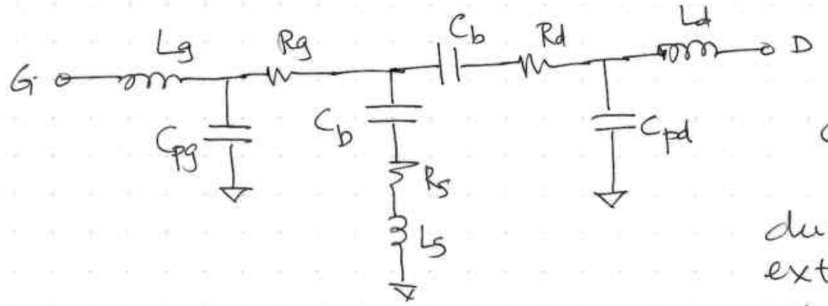
Can use DC measurement to determine R_g, R_d or R_s, or if R_c is known from technology parameters, all unknowns can be solved.

This method does not apply for high-gate metal resistance devices.

MEASUREMENT OF C_{PG} and C_{PD} PARASITIC CAPACITANCES

➤ Bias the FET at $V_{DS} = 0$ and $V_{GS} < V_P$ (below threshold)

The equivalent circuit becomes:



$C_b \rightarrow$ fringing capacitance due to depletion layer extension at each side of gate.

For a few GHz, R/L have no influence on imaginary part of Y-parameters:

(18) ... $Im(Y_{11}) = j\omega(C_{pg} + 2C_b)$

(19) .. $Im(Y_{12}) = Im(Y_{21}) = -j\omega C_b$

(20) ... $Im(Y_{22}) = j\omega(C_b + C_{pd})$

can be solved for C_b, C_{pg} & C_{pd}.

IMPORTANT NOTE ABOUT FREQUENCY

Most of these extractions are done at low frequency where equations (5) - (8) are valid. In this paper, measurements are done in the 1-5 GHz range. If gate length is large, then upper frequency limit has to be reduced for D=1 to be valid. For high frequency devices with short gate length (< 0.3 μ) and short gate width (< 100 μm), Y parameters become ~~too~~ low. Then extractions should be done at higher frequencies where there is less measurement noise in Y-parameters.

After parameters are extracted at low frequency, then the equivalent circuit parameters can be ~~extracted~~ validated over a wide frequency range.